Patent
Attorney's Docket No. 017750-506

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Robert J. MARTIN	)	Group Art Unit: 2878
	)	
Application No.: 09/666,301	)	Examiner: Timothy J. MORAN
	)	
Filed: 21 September 2000	)	Appeal No. *Unassigned*
	)	
For: TWO COLOR QUANTUM WELL FOCAL PLANE ARRAYS	)	Confirmation No.: 8409

SUPPLEMENTAL BRIEF FOR APPELLANT

Mail Stop APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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This Brief is a supplemental brief in response to the Final Office Action mailed 05 September 2003, and includes contents of the Brief filed 03 July 2003. Two extra copies of this supplemental brief are filed herewith.

This appeal is from the decisions of the Primary Examiner dated 14 June 2002 (Paper No. 6) and 05 September 2003 (Paper No. 13), finally rejecting claims 7 and 9-10, which are reproduced as an Appendix to this brief.

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V. Summary of the Invention

Exemplary embodiments of the present invention are directed to a readout circuit that receives charges from a photodector, for example in infrared photodetector. The circuit varies an integration time of moving charges from the photodetector, and includes a first charge well for receiving moving charges from the photodetector, at least one additional charge well, and a mechanism for selectively switching the at least one additional charge well in parallel with

the first charge well to vary the integration time of the moving charges. An exemplary circuit in accordance with the present invention is shown in Figure 2 of the present application.

Employing two or more charge wells in the read out circuit of Figure 2 to vary the integration time, improves the gain and dynamic range of the read out circuit. At long ranges with faint targets, the number of volts per electron becomes a significant factor and signal to noise ratios thus become critical. As a hot target gets closer, the need changes from the need for maximizing the noise to avoiding saturation due to the very large number of target electrons rapidly filling the charge well. The exemplary read out circuit shown in Fig. 2 and encompassed by the present claims solves this problem by augmenting the integration time through a change in the charge well capacitance. This is done via the two charge well capacitances C_{w1} **200** and C_{w2} **205**. Application of a gain switching voltage GN **240** switches in the smaller charge well capacitance C_{w2} **205** to add another twenty decibels of dynamic range to the system's performance. A high total dynamic range performance of 128 decibels can thus be realized (68 dB small well, 40 dB integration time modulation, and 20 dB well change). See, for example, the originally filed specification at page 9, line 19 to page 10, line 4.

VI. The Issues

The issues on appeal are whether claims 7 and 9-10 are unpatentable under:

a) the enablement requirement of 35 U.S.C. § 112, 1st paragraph;

b) the written description requirement of 35 U.S.C. § 112, 1st paragraph; and

c) 35 U.S.C. § 103(a) over U.S. Patent No. 3,624,501 to Joseph ("Joseph").

VII. Grouping of Claims

Claims 7 and 9 stand or fall together. Claim 10 stands separately.

VIII. Argument

A. Claim Grouping

Claim 10 stands separately because it is a method claim and the application is not required to recite structure corresponding to the actions recited in a method claim. In contrast, Claims 7 and 9 are apparatus claims. Claim 10 has different scope and character than Claims 7 and 9, and therefore stands separately from Claims 7 and 9. Furthermore, Claim 7 recites *selectively switching*, whereas Claim 10 recites *selectively varying*. The recitations are different and should be separately evaluated.

B. 35 U.S.C. § 112, 1st ¶, Enablement

In the Office Action, the Examiner rejects Claims 1-11 under 35 U.S.C. § 112, 1st paragraph on grounds the claims are not enabled by the application as originally filed. This rejection is incorrect.

The originally filed specification at page 9, line 23 to page 10, line 2 states:

> *"As a hot target gets closer, the need changes from the need for maximizing the noise to avoiding saturation due to the very large number of target electrons rapidly filling the charge well. The exemplary read out circuit of Fig. 2 solves this problem by augmenting the integration time through a change in the charge well capacitance. This is illustrated in Figure 4 [sic] by the use of the two charge well capacitances C_{w1} 200 and C_{w2} 205. Application of a gain switching voltage GN 240 switches in the smaller charge well capacitance C_{w2} 205 to add another twenty decibels of dynamic range to the system's performance."*

This clearly teaches that the charge well fill rate increases as the target gets closer, and based on the fill rate ("... *the very large number of target electrons rapidly filling the charge well*") the second charge well capacitance is switched into parallel connection with the first charge well capacitance to avoid saturation. In other words, the charge well capacitance is changed to augment integration time as the flow of target electrons increases when a hot target gets closer, so that the large number of target electrons rapidly pouring

into the charge well will not cause saturation. This implicitly discloses changing the capacitance based on the rate of charges flowing from the sensor. Accordingly, the originally filed application teaches *selectively switching the at least one additional charge well in parallel with the first charge well to vary the integration time of the moving charges, based on a rate at which the moving charges fill the first charge well*, as recited in Claim 7, and teaches *selectively varying said integration capacitance to vary the integration time of said moving charges, based on a rate at which the moving charges fill the first charge well*, as recited in Claim 10.

Subtleties of capacitor saturation were well known in the art at the time of the invention, as well as methods of gauging a rate at which a photosensor generates moving charges. For example, as acknowledged by the Examiner in the 05 September 2003 Office Action on page 6, second paragraph, U.S. Patents No. 5,726,045 and No. 4,997,280 teach calculation of a first derivative of a sensor signal, for example a photodetector output signal.

Thus, given the disclosure of the present application (for example the passage at page 9, line 23 to page 10, line 2 cited above, together with the disclosure at page 8, lines 23-25 regarding monitoring the output of the read out circuit of Figure 2 at the end of a time interval), and given the state of the art at the time of the invention as demonstrated for example in U.S. Patents No. 5,726,045 and No. 4,997,280 as well as other references cited and acknowledged in the 05 September 2003 Office Action, the person of ordinary skill in the art at the time of the invention would have been able to make and use the claimed invention. In other words, the person of ordinary skill at the time of the invention would easily have applied such techniques or mechanisms to implement the invention disclosed in the present application to appropriately switch the second charge well capacitance into parallel connection with the first charge well capacitance.

Thus, the originally filed application enables pending Claims 7 and 9-10 and satisfies requirements of 35 U.S.C. § 112, 1st paragraph with respect to Claims 7 and 9-10.

In the *Response to Arguments* section on page 6, first paragraph, the Examiner asserts that implementing the present invention based on the originally filed application would have required a person of ordinary skill in the art to perform undue experimentation. This is incorrect, because such experimentation is predictable, and is commonly performed. For example, when this technology is applied in air combat weapons such as light-seeking or heat-seeking missile systems used to target and destroy aircraft, experimentation is routinely employed to tune performance of such systems given such parameters as light or thermal characteristics of the anticipated target, probable weather or other environmental conditions, aerobatic performance of the missile relative to the target aircraft class, and so forth. Accordingly, those of ordinary skill in the art would thus consider the invention to be claimed described and claimed with sufficient precision to enable them to make and use the invention.

In the *Response to Arguments* section on page 6, second paragraph, the Examiner acknowledges that U.S. Patents No. 5,762,045 and No. 4,997,280 teach calculation of a first derivative of a sensor signal, but asserts that they do not teach that "these signals are used to control capacitance values". Therefore, the Examiner concludes the present claims are not enabled. This conclusion is incorrect because, as explained above, Applicant's present application implicitly discloses using such signals to control capacitance values, for example in the manner recited in the pending claims.

C. 35 U.S.C. § 112, 1st ¶, Written Description

The Examiner asserts that the application as originally filed fails to sufficiently describe the claimed invention to cause one skilled in the art to conclude that the inventor possessed the claimed invention.

This assertion is incorrect, because the person of ordinary skill in the art upon reading the disclosure of the present application would reasonably conclude that the inventor possessed the claimed invention. For example, the passage at page 9, line 23 to page 10, line 2 cited above, discloses changing the charge well capacitance to augment integration time as the flow of target electrons increases when a hot target gets closer, so

that the large number of target electrons rapidly pouring into the charge well will not cause saturation. Thus it would have been clear to the person of ordinary skill in the art upon reading the disclosure of the present application that the inventor possessed the claimed invention.

D. 35 U.S.C. § 103(a), Joseph

In the 05 September 2003 Office Action, the Examiner rejects Claims 7 and 9-10 under 35 U.S.C. § 102(b) over U.S. Patent No. 3,624,501 to Joseph (Joseph).

Joseph discloses an integrating circuit wherein a large capacitor switched out of a parallel connection with a smaller capacitor, thus reducing the integrating capacitance in order to shorten the time constant and thereby allow an easy and rapid initial setting of a rate meter. See for example Joseph at C1/L5-15 (Column 1, Lines 5-15), C1/L21-23 and C1/L63-64. The purpose of this mechanism is to enable a rate meter instrument to be quickly and easily adjusted. The smaller capacitor is used to quickly make adjustments to the instrument, and then the larger capacitor is used for operation of the instrument after it has been adjusted. See, for example, Joseph at C1/L45-49 and C2/L15-18.

Joseph fails to disclose or suggest *selectively switching the at least one additional charge well in parallel with the first charge well to vary the integration time of the moving charges, based on a rate at which the moving charges fill the first charge well*, as recited in Claim 7, and fails to disclose or suggest *selectively varying said integration capacitance to vary the integration time of said moving charges, based on a rate at which the moving charges fill the first charge well*, as recited in Claim 10.

The Examiner acknowledges that Joseph fails to explicitly teach the selective switching of a charge well based on a rate of moving charges, but asserts it would have been obvious to do so "for the advantage of changing the time constant of the device".

This asserted motivation is vague and insufficient to establish a *prima facie* case of obviousness because the Examiner does not explain why this is an advantage, or what would have caused a person of ordinary skill to modify Joseph to incorporate this feature. For example, Joseph discloses only a pushbutton switch SW for switching among the

capacitances, and fails to provide or suggest any rationale or mechanism for automatically switching among the capacitances.

The Examiner appears to be arguing that Joseph can be modified and therefore it is obvious to do so. However, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). In addition, even if a claimed invention is within the capabilities of one of ordinary skill in the art, this is *not* sufficient to establish a *prima facie* case of obviousness. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed.Cir. 1999).

For the above reasons, the Office Action fails to present a *prima facie* case of obviousness with respect to the pending claims.

IX. Conclusion

For at least the foregoing reasons, Appellant respectfully requests that the Examiner's rejections of claims 7 and 9-10 under 35 U.S.C. §§ 112, 1st paragraph and 103(a) be REVERSED.

Respectfully submitted,

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By: _____
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Date: 05 January 2004

APPENDIX A

The Appealed Claims

7. A circuit for varying the integration time of moving charges from a photodetector comprising:

a first charge well for receiving moving charges from a photodetector;

at least one additional charge well; and

means for selectively switching the at least one additional charge well in parallel with the first charge well to vary the integration time of the moving charges, based on a rate at which the moving charges fill the first charge well.

9. The circuit of claim 7, wherein each charge well comprises a capacitor.

10. A method of varying the integration time of moving charges from a photodetector comprising the steps of:

supplying moving charges from a photodetector to an integration capacitance; and

selectively varying said integration capacitance to vary the integration time of said moving charges, based on a rate at which the moving charges fill the first charge well.

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Date: 05 January 2004

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9. The circuit of claim 7, wherein each charge well comprises a capacitor.

10. A method of varying the integration time of moving charges from a photodetector comprising the steps of:

supplying moving charges from a photodetector to an integration capacitance; and

selectively varying said integration capacitance to vary the integration time of said moving charges, based on a rate at which the moving charges fill the first charge well.